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Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

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Washington, D. C. 20231

Case Docket No.0325.00374
Date: June 7, 2000

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): Zhiwu Liu

For: SOFT CODING OF MULTIPLE DEVICE IDS FOR IEEE COMPLIANT JTAG DEVICES

Enclosed are:

1. X Specification (11 pages); Claims (5 pages); Abstract (1 page)

2. X 3 sheets of formal drawings.

3. X Oath or Declaration Total Pages 2
   a. X Newly executed (original or copy)
   b. ___ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Item 5 completed)
   c. ___ Copy of Revocation of Previous Power

4. ___ Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

5. ___ If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

___ Continuation _____ Divisional _____ Continuation-in-part (CIP)
of prior application no.: _____

6. X An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form 1595.

7. ___ A PTO Form 1449 with a copy of the references not previously cited.

8. X Return Receipt Postcard

9. ___ Other:

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Fee	Amount
Basic Fee	--	--	--	$690.00
Total Claims	20	0	x $ 18.00	$ 0.00
Indep. Claims	3	0	x $ 78.00	$ 0.00
Mult. Dep. Claims			$260.00	$ 0.00

SUB-TOTAL $690.00

__ SMALL ENTITY STATUS (divide SUB-TOTAL by two) ..... $ ____

X Assignment Recordal Fee ($40.00) ..... $ 40.00

TOTAL $730.00

X A check in the amount of $730.00 to cover the filing fee is enclosed.

X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

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PATENT TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL561050809US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on June 7, 2000.

By: Mary Donna Berkley
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Respectfully submitted,

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Attorney Docket No.: 0325.00374

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SOFT CODING OF MULTIPLE DEVICE IDS FOR IEEE COMPLIANT JTAG DEVICES

Field of the Invention

The present invention relates to a method and/or architecture for IEEE compliant JTAG devices generally and, more particularly, to a method and/or architecture for soft code for multiple device IDs for IEEE compliant JTAG devices.

Background of the Invention

Implementing JTAG compliant devices on integrated circuits (ICs) is an industry trend. The Institute of Electrical and Electronics Engineers, Inc. (IEEE) publishes a variety of specifications, such as the IEEE 1149.1 standard, published in 1990, which is hereby incorporated by reference in its entirety. An identification (ID) code is an optional instruction in the IEEE 1149.1 standard which requires a device ID (i.e., a 32-bit register). The IEEE standard 1149.1 permits implementation of a single device ID, while remaining in compliance with the JTAG specification.

Referring to FIG. 1, a block diagram of a circuit 10 illustrating a conventional JTAG system is shown. The circuit 10

comprises a logic circuit 12, a multiplexer 14 and a flip-flop 16. The multiplexer 14 has an input 18 that receives the signal from the logic circuit 12 and an input 20 that receives the signal S1. The logic circuit 12 is configured to present either a "1" or a "0" to the multiplexer 14 and cannot be changed. The logic block 12 limits functionality of the JTAG system 10.

The multiplexer 14 also has an input 22 that receives a signal SHIFT. The signal SHIFT selects either the signal received at the input 18 ("0" or "1") or the signal S1 received at the input 20 to be presented to an input 24 of the flip-flop 16. The flip-flop 16 also has a clock input 26 that receives a clock signal CLK. The flip-flop 16 has an output 28 that presents an output signal S0.

When a design is configured to target a single device, the device is assigned an unique device ID. The IEEE 1149.1 specification describes how to implement the unique device ID in a JTAG device. When one design is configured to target multiple devices, the same metal options and bond options are implemented as when targeting a single device. The metal options and bond options are generally considered hard coded.

The logic device 12 is hard coded. Additionally, the hard coded logic block 12 is implemented to provide the device ID. The hard coded device ID logic block 12 (using metal option or bond options) can not be changed after the device 12 has been fabricated. Hard coded device IDs cannot be used in designs which provide multiple configurations using mark options (i.e., no metal options/bond options). Mark inputs can be implemented to provide a configurable device ID, while metal options/band options provide a permanent non-configurable device ID.

Typically, metal options or bond options are used to configure a single design. Conventional JTAG systems implement the same options (metal or bond) to code the ID registers. Device IDs, once hard coded into the ID registers inside JTAG devices, cannot be changed after the device has been fabricated. Conventional hard coded device IDs are not applicable for designs that provide multiple configurations using mark options (no metal options/bond options).

Summary of the Invention

The present invention concerns an apparatus comprising a circuit having one or more inputs. The option inputs may be

configured to provide a device identification (ID) of one or more different device IDs. The one or more inputs may allow implementation of the circuit with one of the one or more different device IDs.

The objects, features and advantages of the present invention include providing a method and/or architecture for soft coding of multiple device IDs for IEEE compliant JTAG devices that may (i) be configured to different device IDs after an integrated circuit (IC) has been fabricated; (ii) be transparent to users; and/or (iii) provide IEEE compliant JTAG devices.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram illustrating a conventional JTAG device;

FIG. 2 is a block diagram illustrating a preferred embodiment of the present invention;

FIG. 3 is a detailed block diagram illustrating an implementation of the present invention in a FIFO; and

FIG. 4 is a detailed block diagram illustrating an implementation of the present invention in a JTAG device.

Detailed Description of the Preferred Embodiments

The present invention provides a method and/or architecture to generate IEEE compliant JTAG devices with unique device IDs that may be used for multiple configuration devices implementing mark options. Certain designs, such as FIFO applications may require IEEE compliant JTAG devices. Certain FIFO designs may not have multiple metal options/bond options configured to handle ID code registers for multiple configuration devices. Therefore, mark options may be implemented in FIFO designs to provide multiple configuration devices. The multiple device IDs required for multiple configuration devices may be provided by the mark options.

Referring to FIG. 2, a block diagram of a circuit 100 illustrating a preferred embodiment of the present invention is shown. The circuit 100 generally comprises a logic circuit 102, a multiplexer 104 and a memory element 106. In one example, the logic block 102 may be implemented as an AND gate. In another example, the memory element 106 may be implemented as a "D" type

flip-flop. However, the logic block 102 and the memory element 106 may be implemented as other appropriate devices in order to meet the criteria of a particular implementation.

The logic block 102 may have a number of inputs 108a-108n that may each receive a signal (e.g., MARKa-MARKn). The signals MARKa-MARKn may be generated externally to the circuit 100. In one example, the signals MARKa-MARKn may be implemented as mark option inputs. In another example, the signals MARKa-MARKn may be implemented as configuration pins. The logic block 102 may present a signal to an input 110 of the multiplexer 104. Additionally, the multiplexer 104 may have an input 112 that may receive a signal (e.g., S1). The multiplexer 104 may also have an input 114 that may receive a signal (e.g., SHIFT). The multiplexer 104 may be configured to present a signal to an input 116 of the memory element 106. The signal SHIFT may select either the signal received at the input 110 or the signal received at the input 112 to be presented to the memory element 106. The signal SHIFT may control the multiplexer 104. The memory element 106 may have an input 118 that may receive a clock signal (e.g., CLK). The memory element 106 may have an output 120 that may present an output signal (e.g., S0). The circuit 100 may allow a single device to

have multiple device IDs while implemented in an IEEE compliant JTAG device.

The external mark options MARKa-MARKn may be used to soft code device IDs. The soft code device IDs may allow a single device to be configured with a number of device IDs. The soft code device IDs may be transparent to customers, while still retaining IEEE 1149.1 compliance in the JTAG specification. The IEEE standard 1149.1 was published in 1990, and is hereby incorporated by reference in its entirety. The following TABLE 1 illustrates soft coding of different mark options (e.g., MARKa-MARKn) for the multiple device IDs:

TABLE 1

MARKa	MARKn	Device	Device ID
GND	GND	5M FIFO	0C402069
VDD	VDD	1M FIFO	0C401069
VDD	GND	¼M FIFO	0C400069

For example, a FIFO may have two mark option pins (e.g., MARKa and MARKn) for configuring the FIFO. The mark pins MARKa and MARKn may allow the FIFO to implement a number of different device configurations/types. The input pins MARKa and MARKn may be

implemented to soft code device IDs as shown in the following TABLE 2:

TABLE 2

MARKa	MARKn	Device	Device ID
0	0	5M FIFO	0C402069
1	1	1M FIFO	0C401069
1	0	¼M FIFO	0C400069

Soft coded device IDs can cooperate with mark options and enable a single device to have multiple device IDs. The circuit 100 may allow the mark options MARKa-MARKn to be transparent to customers. Additionally, the circuit 100 may allow JTAG devices (e.g., the circuit 100) to remain IEEE compliant.

Referring to FIG. 3, an example implementation circuit (or system) 200 of the present invention is shown. The circuit 200 may be implemented as a FIFO memory. The FIFO 200 generally comprises a controller 202. The controller 202 may be similar to the circuit 100. In one example, the controller 202 may be implemented as a JTAG controller. However, the controller 202 may be implemented as another appropriate device in order to meet the criteria of a particular implementation.

The controller 202 may control a configuration (e.g., device ID) of the FIFO 200. The controller 202 may receive a number of signals (e.g., TDI, TCK, TMS and TRST). In one example, each of the signals test data in (TDI), test clock (TCK), test mode select (TMS) and test reset (TRST) may be received from dedicated input pin. In another example, each of the signals TDI, TCK, TMS and TRST may be received from a multi-level input pin. Additionally, the controller 202 may receive a number of mark inputs (to be described in connection with FIG. 4). The controller 202 may generate a signal (e.g., test data out TDO). The signal TDO may indicate a device ID of the FIFO 200. The controller 202 may present a particular device ID (e.g., the signal TDO) in response to the signals TDI, TCK, TMS and TRST.

Referring to FIG. 4, a detailed block diagram of the controller 202 is shown. The controller 202 may have a number of mark input pins (not shown). The mark input pins may allow configuration for a device ID of a particular circuit. Additionally, the mark inputs may be transparent to a user. The controller 202 generally comprises a register 204. The register 204 may be implemented as an identification register. The register

204 may capture bits of data that may identify an ID code of a particular device. Once the ID of the device is captured, the ID code may be shifted out of the register 204 via the pin TDO. The JTAG controller 202 may allow implementation of multiple IDs of a particular device.

The circuit 100 may allow a device to have multiple device IDs. The multiple device IDs may be provided by a number of mark options. The circuit 100 may enable a single physical device to be configured to one of a number of different devices. The multiple configurations may be provided by the mark pins. The circuit 100 may soft code a device ID register and allow a JTAG device to remain compliant with the IEEE standard.

The mark pins may allow the single device to fulfill different customer requirements. The circuit 100 may be configured to different device IDs (e.g., different configurations) after an initial IC fabrication. The circuit 100 may be transparent to customers. The circuit 100 may allow JTAG devices to remain IEEE compliant. The circuit 100 may be implemented to soft code device IDs inside a JTAG device implementing mark options. Additionally, the circuit 100 may be implemented to configured a single device

with multiple device IDs. However, the circuit 100 may require significant design/test overhead.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. An apparatus comprising:

a circuit comprising one or more inputs configured to provide a device identification (ID) of one or more different device IDs, wherein said one or more inputs allow said circuit to be implemented with one of said one or more different device IDs.

2. The apparatus according to claim 1, wherein said device identification ID comprises a soft code.

3. The apparatus according to claim 1, wherein said circuit comprises a JTAG controller.

4. The apparatus according to claim 1, wherein each of said one or more different device IDs comprise a configuration of said circuit.

5. The apparatus according to claim 1, wherein said device identification ID can be configured after fabrication of said apparatus.

6. The apparatus according to claim 1, wherein said circuit comprises:

a logic circuit configured to receive said one or more inputs;

a multiplier configured to receive an output of said logic circuit; and

a memory element configured to receive an output of said multiplexer.

7. The apparatus according to claim 6, wherein said multiplexer is further configured to receive an input signal and a shift signal.

8. The apparatus according to claim 7, wherein said logic circuit comprises a logic gate.

9. The apparatus according to claim 1, wherein said circuit is implemented within a FIFO memory.

10. The apparatus according to claim 1, wherein said one or more inputs comprise mark options.

11. The apparatus according to claim 1, wherein said one or more inputs comprise configuration input pins.

12. The apparatus according to claim 1, wherein said circuit comprises a JTAG device compliant with the IEEE standard 1149.1.

13. An apparatus comprising:

means for receiving one or more inputs; and

means for providing a device identification (ID) of one or more different device IDs, wherein said one or more inputs allow implementation of said one or more different device IDs.

14. A method for multiple device identifications (IDs) comprising the steps of:

(A) receiving one or more inputs; and

(B) providing a device identification (ID) of one or more different device IDs, wherein said one or more inputs allow implementation of said one or more different device IDs.

15. The method according to claim 14, wherein said device identification ID comprises a soft code.

16. The method according to claim 14, wherein each of said one or more different device IDs comprise a circuit configuration.

17. The method according to claim 14, wherein said device identification can be configured after fabrication.

18. The method according to claim 14, wherein said one or more inputs comprise mark options.

19. The method according to claim 14, wherein said one or more inputs comprise configuration input pins.

20. The method according to claim 14, further comprising providing a JTAG device compliant with the IEEE standard 1149.1.

ABSTRACT OF THE DISCLOSURE

An apparatus comprising a circuit having one or more inputs. The one or more option inputs may be configured to provide a device identification (ID) of one or more different device IDs. The one or more inputs may allow implementation of the circuit with one of the one or more different device IDs.

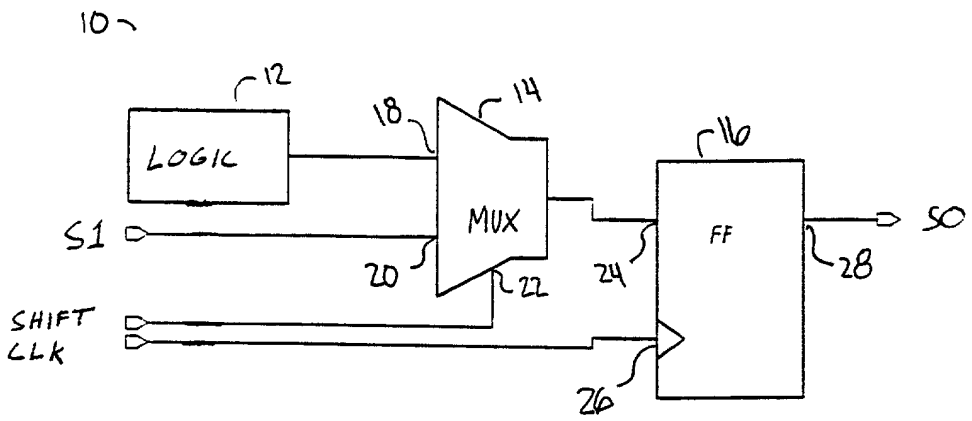
10
12
LOGIC
18
14
MUX
16
FF
S1
20
22
24
28
SO
SHIFT
CLK
26

FIG.1

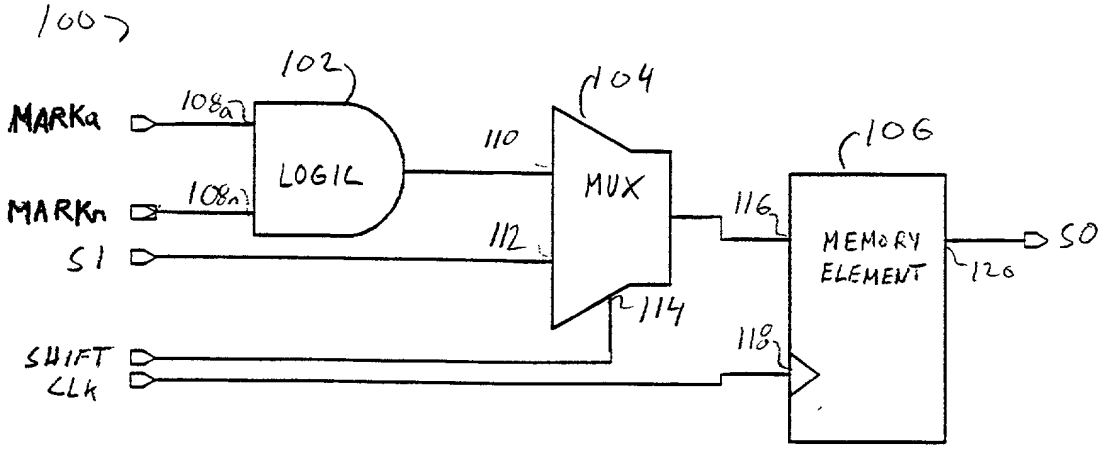
100
102
104
106
MARKa
108a
LOGIC
110
MUX
116
MEMORY
ELEMENT
SO
MARKn
108n
112
S1
114
120
118
SHIFT
CLK

FIG.2

2007

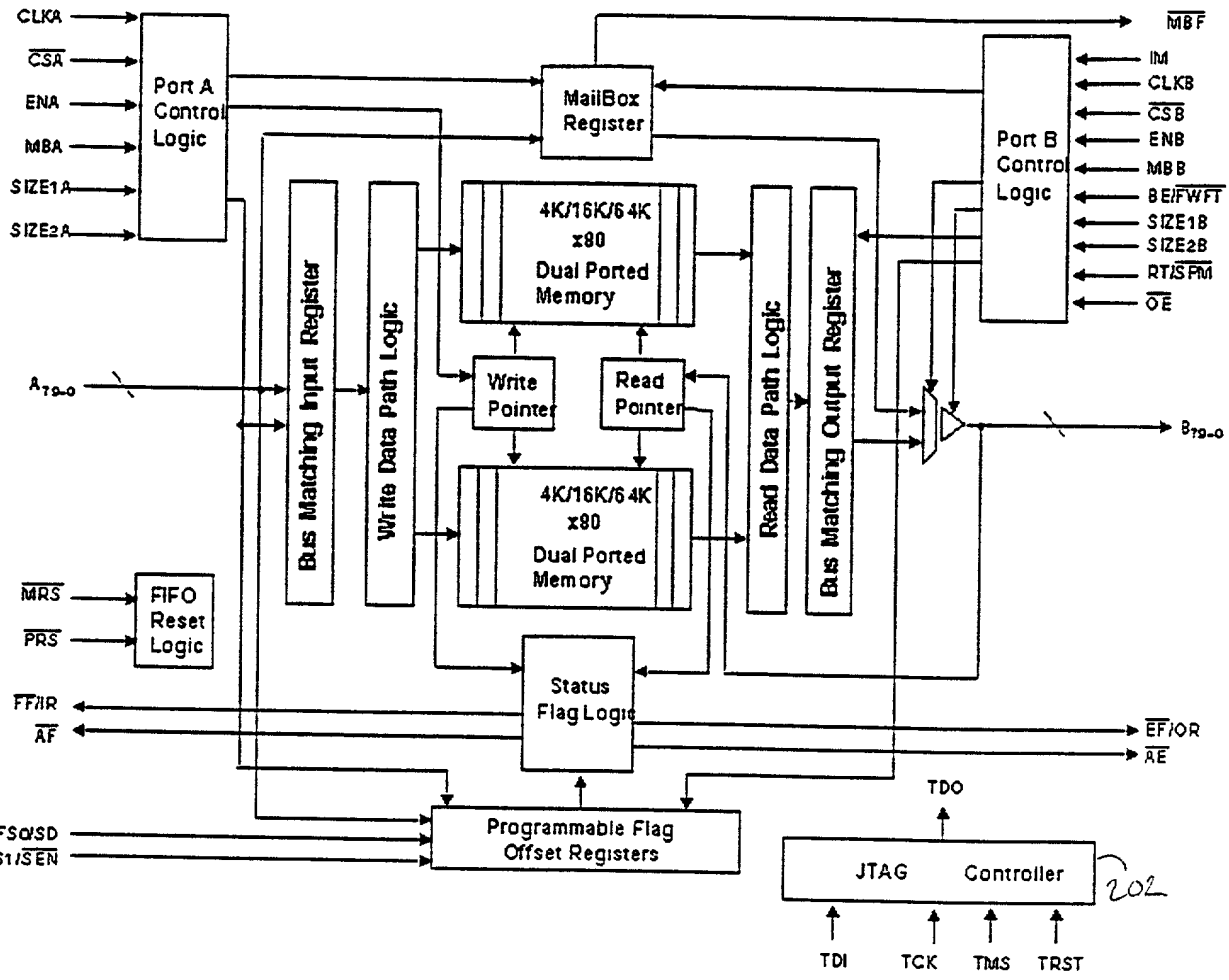
CLKA
CSA
ENA
MBA
SIZE1A
SIZE2A
Port A Control Logic
MailBox Register
MBF
Port B Control Logic
IM
CLKB
CSB
ENB
MBB
BE/FWFT
SIZE1B
SIZE2B
RT/SPM
OE
4K/16K/64K x80 Dual Ported Memory
Bus Matching Input Register
Write Data Path Logic
Write Pointer
Read Pointer
Read Data Path Logic
Bus Matching Output Register
A19-0
B19-0
MRS
PRS
FIFO Reset Logic
Status Flag Logic
FF/IR
AF
EF/OR
AE
FS0/SD
FS1/SEN
Programmable Flag Offset Registers
TDO
JTAG Controller
202
TDI
TCK
TMS
TRST

FIG.3

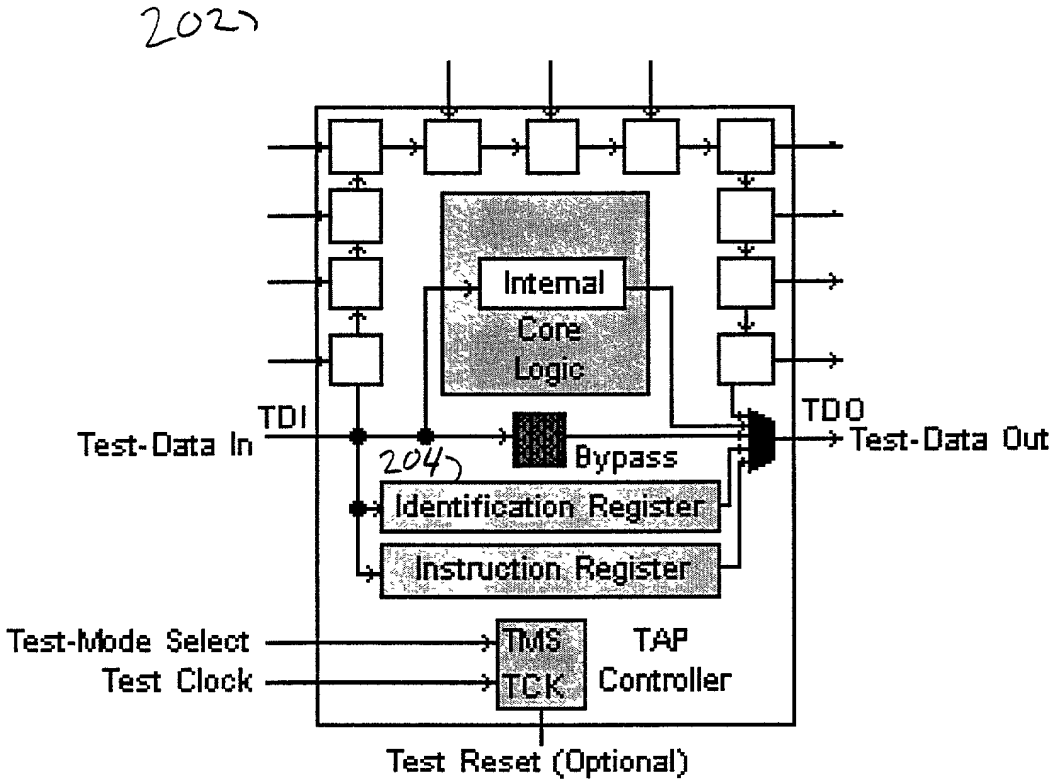

FIG.4

Docket No. 0325.00374

DECLARATION, POWER OF ATTORNEY AND PETITION

I, the undersigned inventor, hereby declare that:

My residence, post office address and citizenship are given next to my name;

I believe that I am the first, original and sole inventor of the subject matter claimed in the application for patent entitled "**SOFT CODING OF MULTIPLE DEVICE IDS FOR IEEE COMPLIANT JTAG DEVICES**", which:

_X_ is submitted herewith;

____ was filed on _____ as Application Serial No. _____ and amended on _____;

I have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

I acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. I also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

> compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or
>
> refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

I hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.	Filing Date

I hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.	Filing Date	Status

Docket No. 0325.00374 Page 2 of 2

I hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.	Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, I acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

I hereby appoint as my attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

21363

PATENT TRADEMARK OFFICE

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

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Signature of Inventor

June 7, 2000
Date

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